Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

CLAIMS:

Please amend claim 1, as follows:

1. (Currently Amended) A computer system for transferring data to a peripheral device, the computer system comprising:

a CPU;

a first memory that may be written to or read by the CPU;

a second memory that may be written to or read by the CPU; and

a DMA controller coupled with the CPU and the second memory, the DMA controller being operable to:

read data from the second memory and transfer the data to the peripheral device,

create a wait state to prevent the CPU from accessing the second memory while the DMA controller is reading data from the second memory,

reconfigure the second memory to prevent the CPU from writing data to the second memory while the DMA controller is accessing the second memory.

enable the CPU to regain access to the second memory once the DMA controller has finished reading data from the second memory, and allow the CPU to access the first memory without delay even while the DMA controller is reading data from the second memory.

2. (Original) The computer system as set forth in claim 1, wherein the DMA controller creates the wait state by suppressing a clock of the CPU while the DMA controller is reading data from the second memory.

3. (Original) The computer system as set forth in claim 1, the peripheral device including a display controller and a display.

4. (Original) The computer system as set forth in claim 1, further including a selector coupled between an address line of the second memory and the CPU and the DMA controller, the selector being controlled by the DMA controller to connect either the CPU or the DMA controller to the address line.

5. (Original) The computer system as set forth in claim 1, further including:

a data bus for transferring data between the CPU and the first memory and the second memory; and

a data bus isolation gate for isolating data lines of the second memory device from the CPU when the DMA controller is reading data from the second memory.

6. (Original) The computer system as set forth in claim 1, further including a selector coupled between the CPU and a read/write line of the second memory, the selector being controlled by the DMA controller to force the second memory to a read state when the DMA controller is reading data from the second memory.

7. (Original) The computer system as set forth in claim 3, the CPU, the second memory, the DMA controller, and the display controller being integrated on a single chip.

8. (Original) The computer system as set forth in claim 1, wherein the first memory and the second memory are formed on separate blocks of RAM.

9. (Original) The computer system as set forth in claim 1, wherein the first memory and the second memory are formed on a single block of RAM that is partitioned into first and second portions.

10. (Original) GPS receiver comprising:

an antenna for receiving GPS signals from a plurality of GPS satellites;

a CPU coupled with the antenna for processing the GPS signals to determine location information for the GPS receiver;

a display coupled with the CPU for displaying at least a portion of the location information;

a first memory that may be written to or read by the CPU;

a second memory that may be written to or read by the CPU; and

a DMA controller coupled with the CPU and the second memory, the DMA controller being operable to:

read data from the second memory and transfer the data to the display,

create a wait state to prevent the CPU from accessing the second memory while the DMA controller is reading data from the second memory,

enable the CPU to regain access to the second memory once the DMA controller has finished reading data from the second memory, and

allow the CPU to access the first memory without delay even while the DMA controller is reading data from the second memory.

11. (Original) The GPS receiver as set forth in claim 10, wherein the DMA controller creates the wait state by suppressing a clock of the CPU while the DMA controller is reading data from the second memory.

12. (Original) The GPS receiver as set forth in claim 10, further including a selector coupled between an address line of the second memory and the CPU and the DMA controller, the selector being controlled by the DMA controller to connect either the CPU or the DMA controller to the address line.

13. (Original) The GPS receiver as set forth in claim 10, further including:

a data bus for transferring data between the CPU and the first memory and the second memory; and

a data bus isolation gate for isolating data lines of the second memory device from the CPU when the DMA controller is reading data from the second memory.

14. (Original) The GPS receiver as set forth in claim 10, further including a selector coupled between the CPU and a read/write line of the second memory, the selector being controlled by the DMA controller to force the second memory to a read state when the DMA controller is reading data from the second memory.

15. (Original) The GPS receiver as set forth in claim 10, further including a display controller for driving the display.

16. (Original) The GPS receiver as set forth in claim 15, the CPU, the second memory, the DMA controller, and the display controller being integrated on a single chip.

17. (Original) The GPS receiver as set forth in claim 10, wherein the first memory and the second memory are formed on separate blocks of RAM.

18. (Original) The GPS receiver as set forth in claim 10, wherein the first memory and the second memory are formed on a single block of RAM that is partitioned into first and portions.

Please add claims 19-24 as follows:

19. (New) A method of controlling access to a memory, the method comprising the steps of:

preventing a memory access device from interfering with the memory, by –

reconfiguring the memory to receive but ignore data from the memory access device, thereby preventing the memory access device from writing to the memory; and

returning control of the memory to the memory access device, by –

reconfiguring the memory to accept data from the memory access device.

20. (New) The method as set forth in claim 19, wherein the memory's data input lines substantially continuously remain effectively connected to the memory access device and the memory's data output lines are effectively isolated from the memory access device while the memory access device is prevented from interfering with the memory.

21. (New) A method of controlling access to a memory, the method comprising the steps of:

writing data from a first memory access device to the memory;

using a second memory access device to gain control of the memory, by –

triggering a first selector to effectively disconnect the address lines of the memory from the first memory access device, and

triggering a second selector to reconfigure the memory to receive but ignore data from the first memory access device, thereby preventing the first memory access device from writing to the memory; and

returning control of the memory to the first memory access device, by –

triggering the first selector to reconnect the memory's address lines to the first memory access device, and

triggering the second selector to reconfigure the memory to accept data from the first memory access device.

22. (New) The method as set forth in claim 21, wherein the memory's data input lines substantially continuously remain effectively connected to the first memory access device and the memory's data output lines are effectively isolated from the first memory access device while the second memory access device controls the memory.

23. (New) A method of transferring data to a display, the method comprising the steps of:

reading data from a first memory to a CPU;

writing data from the CPU to the first memory;

writing data from the CPU to a second memory;

updating the display using a DMA controller to gain control of the second memory, by –

triggering a first selector to reconfigure the second memory's address lines from the CPU to the DMA controller, thereby effectively disconnecting the address lines of the second memory from the CPU and connecting the address lines of the second memory to the DMA controller, and

triggering a second selector to reconfigure the second memory to receive but ignore data from the CPU, thereby preventing the CPU from writing to the second memory; and

returning control of the second memory to the CPU, by –

triggering the first selector to reconfigure the second memory's address lines from the DMA controller to the CPU, thereby effectively disconnecting the address lines of the second memory from the DMA controller and connecting the address lines of the second memory to the CPU, and

triggering the second selector to reconfigure the second memory to accept data from the CPU.

24. (New) The method as set forth in claim 21, wherein the second memory's data input lines substantially continuously remain effectively connected to the CPU and the first memory and wherein the second memory's data output lines are effectively isolated from the CPU while the display is being updated.

No new matter has been introduced as a result of these changes.